Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-2. (canceled)

3. (currently amended) The method of claim 21~~1~~ wherein the ferroelectric material is a PZT bearing compound.

Claims 4-5. (canceled)

6. (currently amended) The method of claim 21~~1~~ wherein the ferroelectric material has a thickness of less than about 1,000 Angstroms.

7. (canceled)

8. (currently amended) The method of claim ~~1~~21 wherein the ferroelectric material has a thickness of about 100 Angstroms and greater.

9. (currently amended) The method of claim 21~~1~~ wherein the ferroelectric material is PZT.

Claims 10-13. (canceled)

14. (currently amended) The method of claim ~~1~~21 wherein the ferroelectric material is highly oriented.

15. (canceled)

16. (currently amended) The method of claim ~~1~~21 wherein the ferroelectric material is substantially free from an amorphous structure.

Claims 17-18. (canceled)

19. (currently amended) The method of claim ~~1~~21 wherein the oxide layer is provided by a dry oxidation process comprising an oxygen bearing compound.

20. (currently amended) The method of claim ~~1~~21 wherein the oxide layer passivates the surface of the substrate to protect the channel region.

21. (Currently Amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming a gate oxide layer on the substrate, the oxide layer having a non-crystalline structure;

forming a MgO layer on the oxide layer after forming the oxide layer on the substrate, the MgO layer having a crystal structure;

thermally annealing the MgO layer to enhance an alignment of crystallites of the MgO layer;

forming a ferroelectric material overlying the substrate and the MgO layer;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region, wherein the gate oxide layer is a first buffer layer and the MgO layer is a second buffer layer,

wherein the MgO layer formed on the oxide layer is provided with a highly-oriented structure prior to the annealing step,

wherein the MgO layer has a polycrystalline structure prior to the annealing step.

22. (canceled)

23. (Currently Amended) The method of claim 21, wherein the oxide layer has an amorphous structure ~~and the MgO layer has a crystal structure~~.

24. (Original) The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.

25. (canceled)

26. (Original) The method of claim 21 wherein the second buffer layer is thermally annealed at a temperature of 800-1000 degrees Celsius.

Claims 27-31. (canceled)

32. (currently amended) A method for fabricating a non-volatile memory device, the method comprising:

providing a semiconductor substrate;

forming an amorphous gate dielectric layer on the substrate;

forming a MgO layer on the amorphous dielectric layer after forming the dielectric layer on the substrate, the MgO layer having a highly-oriented structure; and

forming a ferroelectric layer overlying the MgO layer,

wherein the dielectric layer, MgO layer and ferroelectric layer are patterned to form a transistor,

<u>wherein the MgO layer has a polycrystalline structure</u>.

33. (canceled)

34. (canceled)